

King Fahd University of Petroleum and Minerals
Electrical Engineering Department

EE200: Digital Logic Circuit Design
Course Coordinator: Dr. Mahmoud M. Dawoud
First Semester 2005-2006 (051)

A. Course Information

Text Book:		Digital Design (3rd Edition) by M. M. Mano			
Course	Name	Office	Phone	Sections	
Coordinator:	Dr. Mahmoud M. Dawoud , <i>mmdawoud@kfupm.edu.sa</i>	14/277	2299		
Instructors:	Your Section Instructor is:				
Lab	Name	Office	Phone	Sections	
Coordinator:	Mr. Ahmed Abul Hussain, <i>ahussain@kfupm.edu.sa</i>	26-255	1241		
Instructor:	Your lab. Instructor is: _____@kfupm.edu.sa				
Grading:	Assignments and Quizzes	Laboratory	Design Project	Two Majors	Final
	15%	20%	5%	30%	30%
	First Major	Second Major	Lab Final	Final	
Exams Dates:	Sat. October 15, 2005	Sat. December 17, 2005	December 24-28, 2005	Per the schedule from the registrar's office	
Exams Times:			Your Lab time		
Exams Places:			In your Lab		
Important Dates:	Last day to drop the course without a permanent record	Last day to drop the course with "W" grade	Last day to drop all courses with "W" Thru Registrar's office.		
	September 20, 2005	October 25, 2005	November 30, 2005		

- Note #1:** Final Exam is **coordinated** and **comprehensive** (i.e. it is common for all sections and covers chapter 1-7 as described in the syllabus and class notes). Lab Final will be given by the Lab instructor in the Lab during the normal Lab session.
- Note #2:** According to the rules and regulations of KFUPM, attendance is **MANDATORY**. More than **8** unexcused absences will be reported to the registrar office and result in a **GRADE of DN** regardless of the student's grade.
- Note #3:** It is your responsibility to solve the *practice problems* as soon as the material is covered in the class. Solution will be posted on **WebCT**. This *practice problems* set will not be collected.
- Note #4:** Your instructor will give you other home work assignments which will be collected and graded. Quizzes will be given regularly based on the homework and the *practice problems*.
- Note #5:** A design project will be assigned around week 11 and will be due at the end of week 13.
- Note # 6:** **On-line lectures will be available under WebCT which is maintained by the course coordinator. All students will have access to these lectures. All students are encouraged to access these lectures before attending the regular classes. A feed-back will be obtained from the students through questionnaires.**
- Note # 7:** **Weeks 5, 6, and 7 will be conducted fully on-line. You will study the material on-line. You will communicate with your instructor via WebCT communication tools. You will attend Wednesday classes of these weeks. In Wednesday class, you will have the chance to discuss the material and take a special quiz.**

B. Tentative Course Outline and Schedule

Week	Date	Topics	Sections	Labs/Prob. Sessions
1	September 10-14	Binary Numbers, Number Base Conversions,	1.1-1.3	No Lab.
2	September 17-21	Octal & Hexadecimal Numbers, Complements, Signed Binary Numbers, Binary Codes	1.4-1.7	Introduction to Lab. Equipment, Exp#1: Binary & Decimal Numbers
3	September 24-28	Binary Logic, Boolean Algebra: Axioms, Theorems & Properties. Boolean functions, Digital Logic Gates	1.9, 2.1-2.4 2.7-2.8	No Lab.
4	October 1-5	Canonical & Standard Forms, More Logical Operations, Simplification of Boolean functions Using K-Maps, Product of Sums Simplification.	2.5-2.6 3.1-3.4	Exp#2: Digital Logic Gates
5	October 8-12	Don't-care Conditions, NAND, NOR, and Other Two Level Implementations, Exclusive-OR Function, Introduction to HDL.	3.5-3.8	Exp#3: Introduction to LogicWorks
6	October 15-19	Combinational Logic: Analysis and Design Procedures, Code Conversion, Adder circuits.	3.9, 4.1-4.4	Exp#4: Boolean Algebra Exam # 1
7	October 22-26	Subtractors, Decimal Adder, binary multiplier, Magnitude Comparator, Decoders.	4.5-4.8	Exp#5: Simplification
Eid Al-Fitr Vacation				
8	November 12-16	Encoders and Multiplexers, Random Access Memory.	4.9-4.10, 7.2, 7.3	Exp#6: Code Conversion
9	November 19-23	Programmable Logic, PLD'S, ROM, Programmable Logic Array, Programmable Array Logic.	7.5-7.7	Exp#7: Adders/Subtractors
10	November 26-30	Sequential Circuits, Latches, Flip-flops, Characteristic Tables	5.1-5.3	Exp#8: Multiplexers
11	December 3-7	Analysis of Clocked Sequential Circuits, State Reduction and Assignment.	5.4, 5.6	Exp#9: Design with ROM's
12	December 10-14	Flip-flop Excitation Tables, Design Procedure, Synthesis using different flip flops.	5.7	Exp#10: Flip-flops
13	December 17-21	Registers and Shift Registers	6.1, 6.2	Exp#11: Counters & Sequential Logic Exam # 2
14	December 24-28	Ripple Counters, Synchronous Counters and other counters.	6.3-6.5	Lab Final
15	December 31 - January 4	Revision		

C. Practice Problems

Chapter 1: 5,7,9,18,20,29,34
Chapter 2: 2,5, 9, 12,15,17
Chapter 3: 2,7,12,15,19,24,31,36
Chapter 4: 5,11,13,20,25,29,31,35,37
Chapter 7: 15,18,20,21,24
Chapter 5: 2,6,9,12,19, 24,26
Chapter 6: 5,7,8,12,21